A NEW POWER MODULE PACKAGING TECHNOLOGY FOR ENHANCED THERMAL PERFORMANCE

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INTRODUCTION

The emerging advanced power device technologies Integhrated Gate Bipolar Transistor (IGBT), Metal Oxide Semicondustor Field Effect Transistor (MOSFET), MOS Controlled Thyristor (MCT) are pushing the current densities, switching speeds and frequencies to new dimensions (Hingorani, 1993). To fully utilize the capabilities of such devices there is a need to provide the electrical, structural and thermal environments compatible with their packaging requirements In response to these needs, GE CR&D Center developed the Chip on Flex Power Overlay (POL) technology which can be combined with a double sided integral compact heat exchanger technology. This advanced power modules technology offers significantly improved thermal and electrical performance for a broad range of commercial and military applications in a wide range of power levels (Ozmat , 1997, 1998)

The POL and integral heat exchanger based andvanced power module technology can reduce the Rjc-junction to case and Rja-junction to ambient thermal resistances to 0.04 ^{o}C/W and 0.05 ^{o}C/W for an 1in^{2} base area, respectively. The low thermal resistance is due to eliminating the resistive interfaces, providing double sided cooling capability, and a large surface area and improved film coefficient.

AN OVERVIEW OF POL TECHNOLOGY.

Typical state of the art commercial power module designs employ wire bonds for connecting power devices to power busses and control terminals. The power devices are commonly soldered onto a metalized insulating ceramic substrate, often beryllium oxide or aluminum nitride metalized with direct-bond copper and large-area-solder bonded to a massive copper heat spreader. Typically, an injection molded polymer shell covers the module, exposing only the input/output and control terminals and the copper heat spreader. The heat spreader is attached to a heat sink, such as extruded aluminum fins or a cold plate, for example. Thermal contact between the heat spreader and the heat sink is achieved through a thermal paste or a thermally conductive polymer, (Sorgo, 1996).

Disadvantages of power module designs such as those described here in above include high parasitic impedance (Tsai, 1995), high volume and weight, high thermal resistance, and limited reliability due to bond wires. Accordingly, it would be desirable to provide a power electronic module packaging technology, which overcome these disadvantages.

The advanced POL technology offers significant advantages over the state of the art power modules available on the market to day, as described above. Higher packaging density, lower package parasitics, higher reliability, lower weight and size and higher efficiency are among the key advantages of this technology.

The POL technology eliminates bond wires. The power and control circuits to device interconnections are achieved through metalized through holes. This approach dramatically reduces the interconnect length, interconnect parasitics, and increases packaging density by allowing us to pack power devices more closely.

An extremely important feature of the POL is the capability of double sided cooling with or without integral heat exchanger. Thermally, the approach creates a planar interface that makes it possible to remove the heat from the topside of the module as well as the bottom side. The low thermal resistance of the top side path between the heat sink and the top layer of the power devices where most of the heat generation takes place offers improved thermal performance compared to cooling through the back side of power devices alone. For example, 90% of the power dissipation is in the upper 10% of a power MOSFET device. It is also now possible to employ double sided cooling which can more than double

the thermal performance of power module. Therefore, the improved thermal performance strongly couples with and complements the no wire bond approach allowing us to take full advantage of the POL technology.

As a result of these two key features and fully striplined power electrode design the module EMI will be significantly lowered and the module efficiency will be improved. A natural outcome of these enhancements is the ability to switch the advanced power devices at higher speeds and frequencies without pushing the limits of Safe Operating Area (SOA) of power devices. The reduced electrical parasitics, particularly reduced L di/dt noise will allow us to use power devices with lower breakdown voltage, which improves both the cost and the electrical efficiency of modules. Ultimately the size, the weight and the cost of passive filter components will also go down which helps us to meet the requirements of advanced power modules for commercial and military applications more effectively.

A COST EFFECTIVE APPROACH TO POL FABRICATION PROCESS

The POL technology is designed to make use of the commercially available materials, processes and equipment wherever possible. The manufacturability, cost and reliability factors have been incorporated early in the design. The following paragraphs describe the various steps of the POL fabrication process.

As illustrated in FIG. 1, The first step is to attach a single layer dry polymer film to a carrier frame, usually a circular or square shaped metal ring, through a bond layer.

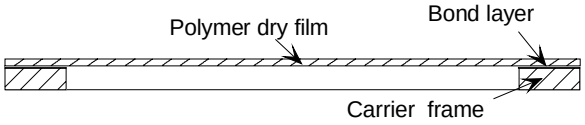

Figure 1. A thin film of polymer is attached to a carrier frame

The dry polymer film is a suitable dielectric material, such as a polyimide film; Kapton sold by E.I. DuPont de Nemours and Company. The polymer layer is flat and stretched which is required for further processing. The polymer layer stretches during the cool down cycle of the frame attach process, a lamination process. Curing of the bond layer takes place at high temperature (up to 300 ^{o}C) and pressure (several hundreds of psi) in a lamination press. Since the metal frame has a lower Coefficient of Thermal Expansion (CTE) than that of the polymer, polymer layer remains in a stretched state after the cool down to room temperature. The carrier frame provides a convenient way for transport, ease of handling and dimensional stability.

Figure 2 illustrates stepping and punching a via pattern in the polymer film which forms the device power and control connections. Forming the via pattern can be accomplished by mechanical punching or laser processing. Increased via density advantageously reduces resistive losses and current crowding. An exemplary configuration comprises 0.020 inch diameter vias on 0.050 inch staggered centers.

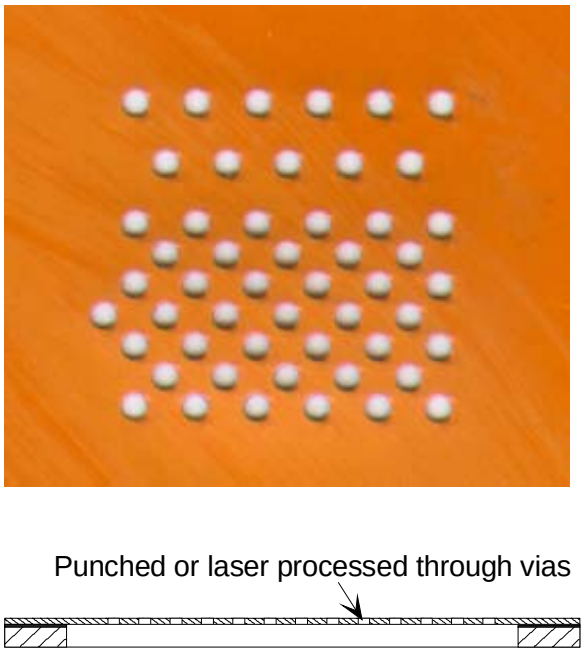

Figure 2. Through vias are formed in the membrane by punching or laser processing.

Figure 3 illustrates applying a partially cured polymer resin (e.g., acrylic or epoxy) over the topside of the membrane as a bond, or glue, layer. An exemplary bond layer is approximately 0.0005 inch thick. Application of the bond layer may take place before or after the hole formation process. A protective release layer is applied over the glue layer

Which keeps the sticky bond layer clean during the via formation process.

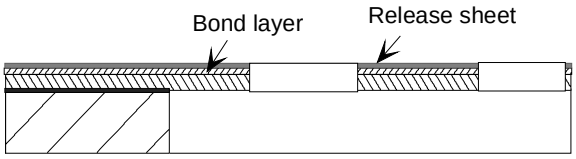

Figure 3. A partially cured B-stage bond layer protected by a release layer,

Figure 4 illustrates placing power devices on the bond layer. Two devices are provided by way of example only. In order to bond the devices, the structure is cured in a vacuum oven under low pressure. During the curing process, some resin from the bond layer may be extruded into the punched holes (or vias), resulting in a ring of cured resin covering the device metalization about each hole.

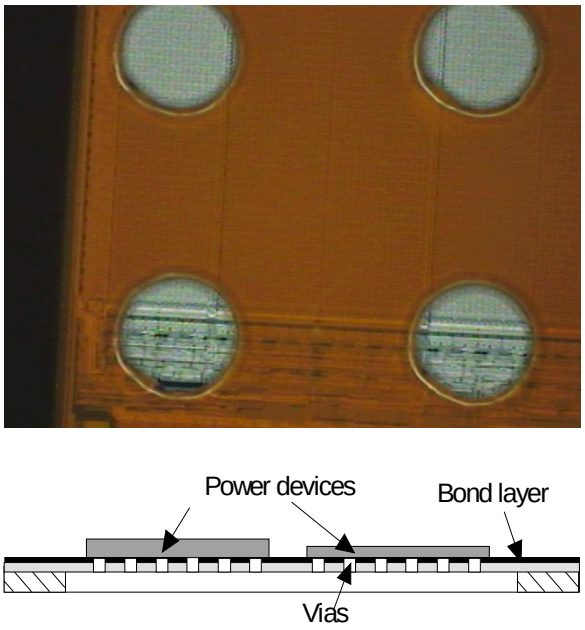

Figure 4. Power devices are picked, aligned and placed over a partially cured B-stage bond layer. To achieve permanent bonding the assembly is then cured in a vacuum oven.

Figure 5 below illustrates sputter-cleaning the residual bond layer and a thin layer aluminum oxide from the top layer metalization (e.g., aluminum) of typical power devices. Since Al readily oxidizes at standard atmospheric conditions, removing the non-conductive oxide layer prior to subsequent metalization processes is necessary. Blanket sputtering of a layer of adhesion metal and a layer of conductive seed metal layer over the aluminum follows the cleaning process. Suitable adhesion and conductive metal layers comprise a couple of thousands of angstroms thick titanium and copper, respectively. Subsequently, a conductive copper layer (e.g., approximately 0.002 inch to 0.010 inch thick) is electroplated over the sputtered seed copper layer. The plated blanket copper layer is then subtractively patterned to form the power and control circuit and their input/output pads. Another alternative is to form the power circuit by semi-additively where selective electroplating to the desired Cu thickness is accomplished through an exposed and developed photoresist. The thin layer of adhesion and seed layer will be then removed by blanket etching the circuit. The patterned Cu land and traces are subsequently plated with an approximately 200 μ" thick electroless Ni followed by an approximately 10 μ" thick electroless Au layers (Parquet, 1996).

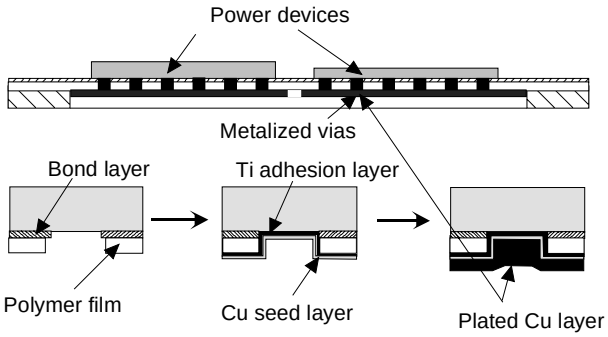

Figure 5) Remove the cured bond layer by RIE, sputter clean the metal contacts, sputter Ti and seed Cu layer, electroplate plate with Subtractively or semi additively form the desired pattern.

As shown in FIG. 6 and 7, the power devices are connected to an electrically insulating, but thermally conducting, base plate An exemplary base is fabricated by metalizing an aluminum nitride plate (e.g., approximately 0.040 inch thick) by copper and CuMo30 which is a composite material made by infiltrating porous Mo base with Cu over the upper and lower surfaces, respectively. The solderable backside metalization of the power devices is bonded to copper metalization of the power circuit formed over the aluminum nitride thermal base. The second layer of the power circuit is fabricated by directly active-brazing one or more physically separated layers of copper sheets, each having a

different thickness with respect to the aluminum nitride thermal plate. The copper sheets are over-sized with respect to the underlying AlN plate. The over-sized copper sheets are etched to provide a design-specific pattern having three levels of thickness, including zero thickness, the full thickness of the original copper sheet, and a fractional thickness of the original copper sheet(s). The selective etching process is preferably performed in multiple steps that will provide the circuit pattern and the desired thickness variations. The thickness variations accommodate variations in thickness of different types of power devices fabricated by different manufacturers. For example, thickness variations of 0.015 inch can be accommodated in a step-wise fashion. The screened and re-flowed solder thickness (approximately 0.003 inch, for example) help to accommodate statistical variations in thickness of power devices and thickness of the etched layers, both of which are usually less than +/- 0.001 inch.

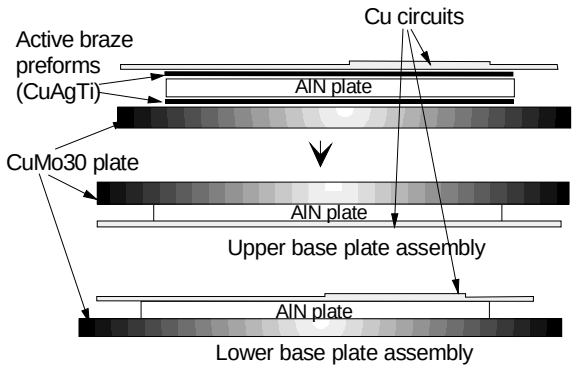

Figure 6) Insulating thermal base fabrication: Active brazed partially and fully etched Cu and CuMo30 composite sheets on upper and lower AlN base plates

Advantageously, due to the planarity, this structure provides a double-sided cooled module design. Double-sided cooling takes advantage of the planarity of the top (first) layer of the power circuit. The top layer power circuit can be mirror-imaged on an oversized copper sheet of the upper thermal base assembly that is actively brazed to an aluminum plate, as described above. Since such copper metalization can carry the required current levels, the thickness of the plated-up Cu layer may be significantly reduced. The metalized and patterned membrane carrying the power devices are then situated between the copper-metalized aluminum nitride sheets and soldered in a single or two step, fluxless soldering process in a reducing atmosphere.

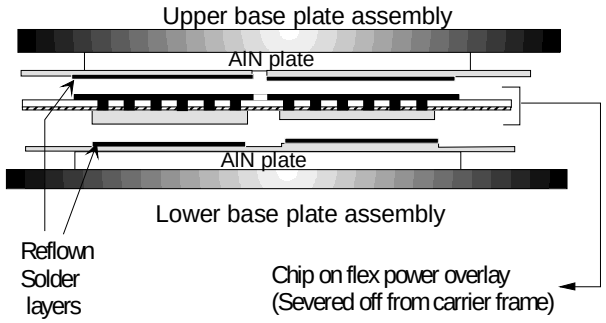

Figure 7) POL is placed between the upper and lower base plate assemblies and reflown to form the power circuit.

For a non-hermetic commercial power module design, the copper-metalized aluminum thermal plates are attached to infiltrated CuMo30 composite plates. An exemplary thickness of copper-molybdenum plates is in the 0.050 inch to 0.100-inch range, as determined by the module size and stiffness requirements. The copper-molybdenum sheets and the integral-reticulated, metal-based, compact, high performance heat exchangers are bonded to aluminum-nitride thermal plates prior to the solder attach process, as illustrated in FIG. 8.

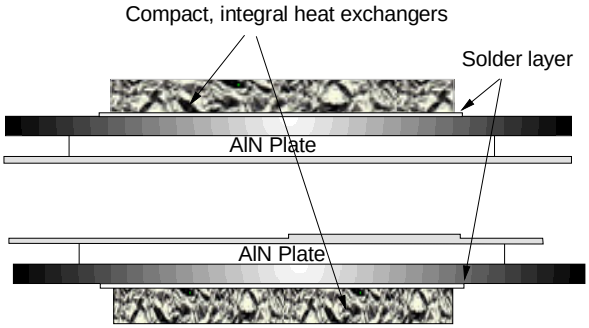

Figure 8) Heat Exchangers are solder attached to upper and lower base subassemblies

Upper and lower enclosures seal the liquid or gaseous coolant against CuMo plates by module clamping screws Figure 8. Upper and lower base plate subassemblies are separated from each to

provide the exact spacing needed by the thickness of POL and the bonding solder layers.

This separation distance is controlled by expansion matched spacers as shown in Figure 9. All critical interfaces of COF POL solder joints and brittle semiconductor devices are protected against shear and normal loads by the rigid structure formed by CuMo plates and the spacer.

Furthermore, the lower coolant enclosure and base plate subassembly is contained in a cavity providing damping and stress isolation against external loads. A metalized and patterned extension of the dielectric film carrying the POL is formed to provide stress relieved connections to gate control circuits and external connectors, which are integrated to the upper coolant enclosure as shown in Figure 9.

The upper coolant enclosure contains slots for power electrodes go through and form external power bus connections. Capture nuts, embedded in the upper coolant enclosure help to form secured and reliable connections to the external power bus.

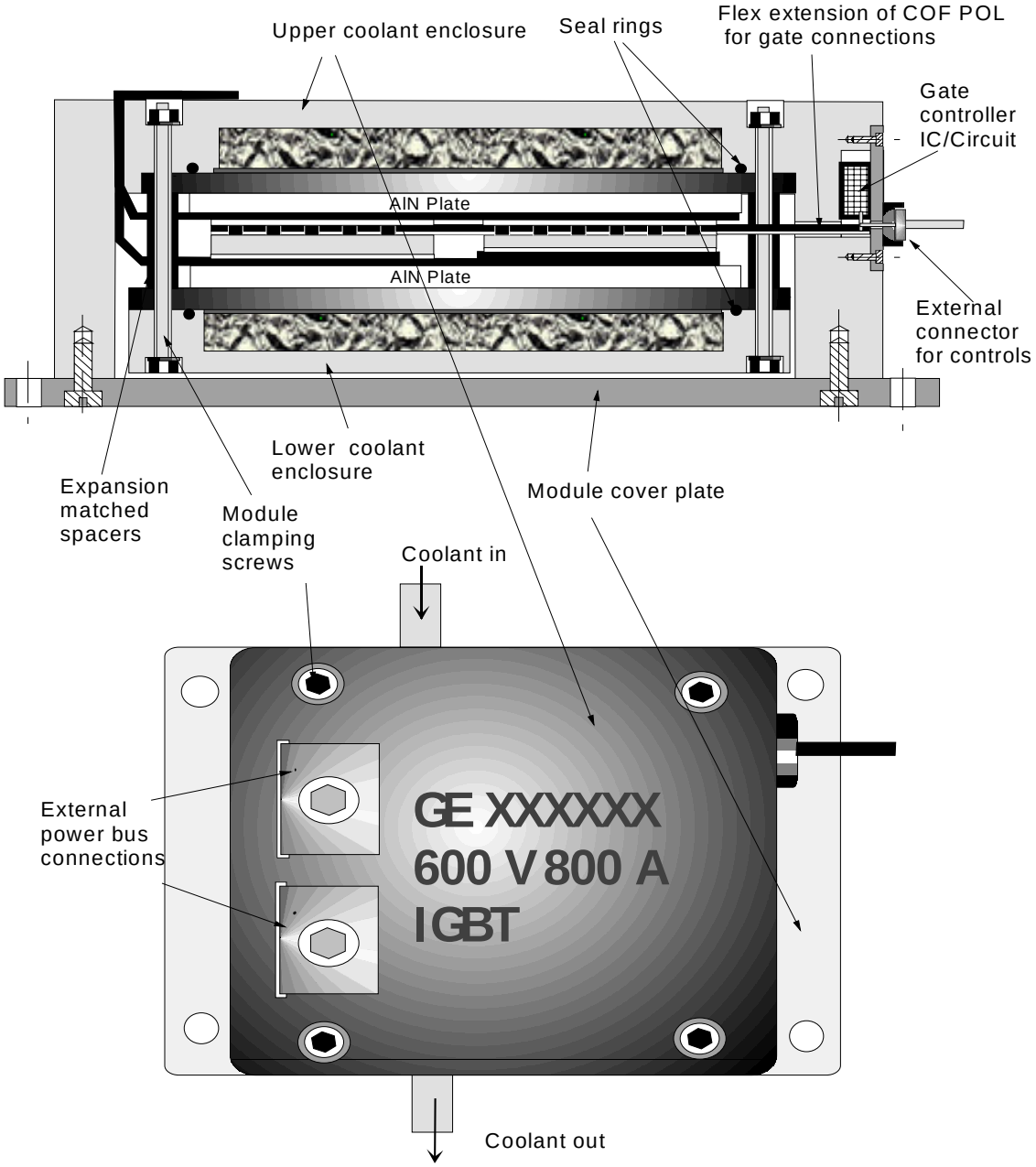

Figure 9. A cross section and top view of a non-hermetic double sided cooled POL based power module withintegral heat exchangers.

THERMAL CHARACTERISTICS OF POL MODULE.

The GE POL combined with an integral high performance heat exchanger offers significant thermal advantages over the state of the art power modules.

The stack up of the POL technology provides low resistance thermal paths for the top, bottom and double sided cooling approaches.

Since POL eliminates the bond wires, and thereby offers a planar structure the top sided cooling becomes feasible. The majority of power dissipation takes place in the top 10% of the devices. The thermal path between the ambient and where the heat is being generated becomes shorter, and as a result the thermal resistance is significantly reduced.

The improved thermal performance combined with the POL technology offers significant reliability, cost, electrical performance, size and weight advantages for the power modules.

Since the heat removal becomes much less of an issue, the power devices can now be brought to close proximity of each other. The reduced path length between the devices reduces parasitics inductance and resistance of power module. As a result, faster switching becomes possible which reduces the size, weight and the cost of passive filter components. Since the L.di/dt noise is reduced, the module may use power devices with lower voltage rating, which lowers the cost and increases the efficiency of power modules.

To quantify the thermal advantage of POL technology 3D Finite Element (FE) technique was used. Thermal performance of a power module with (4) MOSFET devices was modeled. Due to the symmetry of the geometry, only a quarter of the module was analyzed. The FE model was developed for two different device pitches, a compact 0.050" pitch and a relaxed 0.250" pitch. The purpose was to show the effect of spreading on the thermal performance of the POL technology.

The physical dimensions of the power MOSFET device are 0.300 inch x 0.300 inch x 0.022 inch. The device was rated for 100 W/cm^2 dissipation. It was assumed that the 90% of the dissipation were taking place in top 10% thickness of the device. The total dissipation level is 40W/device in the active area of about 0.250 inch x 0.250-inch size.

A cross section of the thermal model with various interfaces and material layers is shown in Figure 10 for a typical POL design. Table 1 below summarizes the thickness and the material properties of each layer.

The stack up uses two Cu metalized AlN plates that are identical in size. It was assumed that the Cu was bonded to AlN layer by active brazing or by Direct Bond Copper (DBC) approach. Figures 11 and 12 show the FEM built for the POL structure.

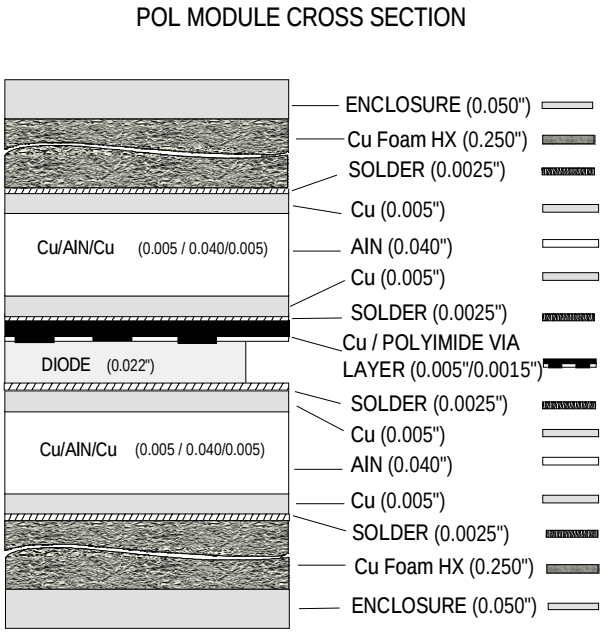

Figure 10. A cross section of the 3D FEM of POL

Two different boundary conditions were applied to FE models to calculate the junction to casing (R_{jc}) and junction to ambient (R_{ja}) thermal resistance for double sided, top side and bottom side cooled cases. For the R_{jc} case the top and bottom surface temperatures were fixed at 0 ^oC. For the R_{ja} case the effective convection film coefficient was taken as 40 W/in^2-^{o}C. The effective film coefficients and surface area multiplier factors were used in modeling the convective aspects of the heat transfer. It was assumed that the film coefficient h is 1 W/^{o}C/cm^2 (Mahalingam, 1985), and the effective surface area multiplier is 6 for the high performance integral compact heat exchanger. This value was

experimentally shown to represent the integral reticulated Cu foam based heat exchangers using 40 ppi and 40 % dense Cu foam soldered to the Cu metalized AlN thermal base (Ozmat, 1998). The FE Analysis was performed for two different device separation values, 0.050 inch and 0.250 inch for all cases. The via layer design used filled vias with 0.020 inch diameter in 0.050 inch staggered pitch configuration

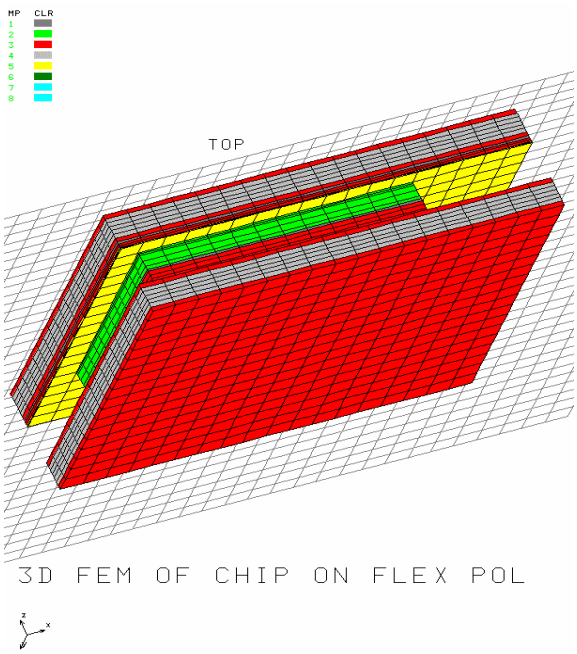

Figure 11. A 4 fold symmetry based FEM of the POL structure tilted to show the MOSFET and PI-Via layers.

Material	Thickness (Inch)	K_{th} (W/in-C)
Active Brazed Cu	0.0050	9.8
AlN	0.0250	4.5
Active Brazed Cu	0.0050	9.8
Solder	0.0025	1.0
Plated Cu	0.0050	9.8
Polyimide-via	0.0015	2.5
Silicon	0.0220	2.5
Solder	0.0025	1.0
Cu post	0.0200	9.8
Solder	0.0025	1.0

Table 1. The thickness and thermal conductivity of materials used in the 3D FEM model of POL

The typical temperature distributions as predicted by the FEA in the POL modules are shown in Figures 12 and 13. The table 2 summarizes the results of 12 different cases analyzed.

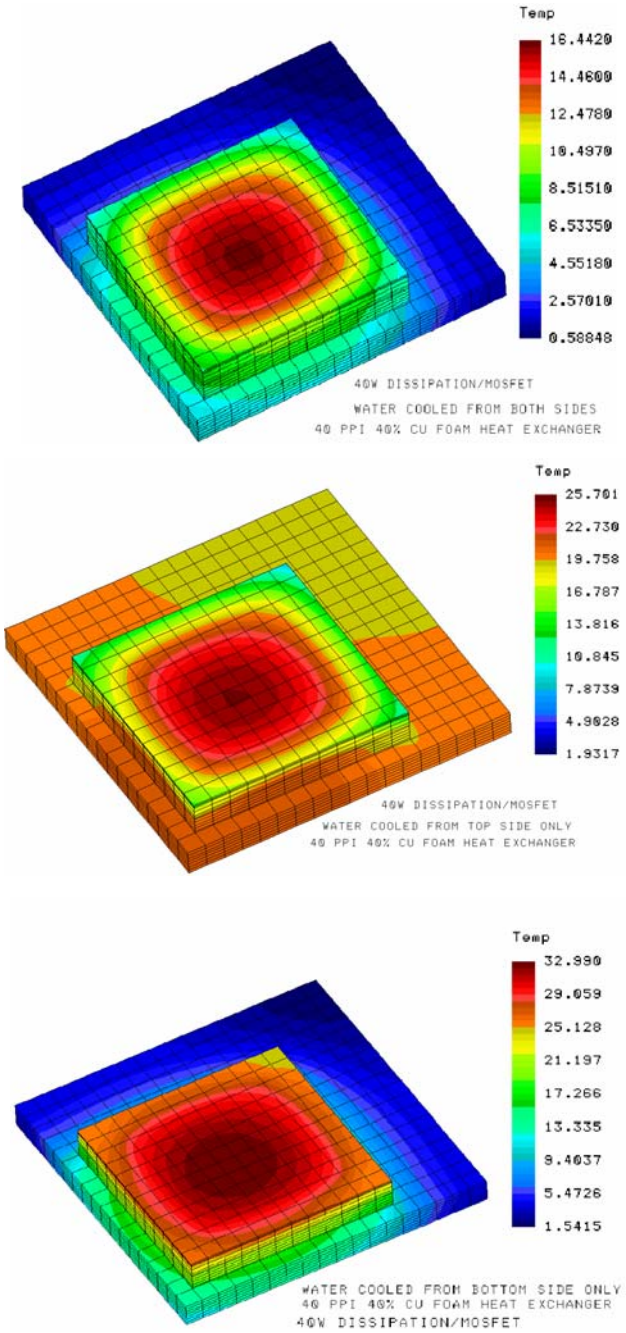

Figure 12. Temperature distributions in the POL modules as predicted by 3D FEA. The device pitch is 0.050 inch. The module is water cooled by a foam based integral heat exchanger from both sides (upper), from top side only (middle), and from bottom side only (lower).

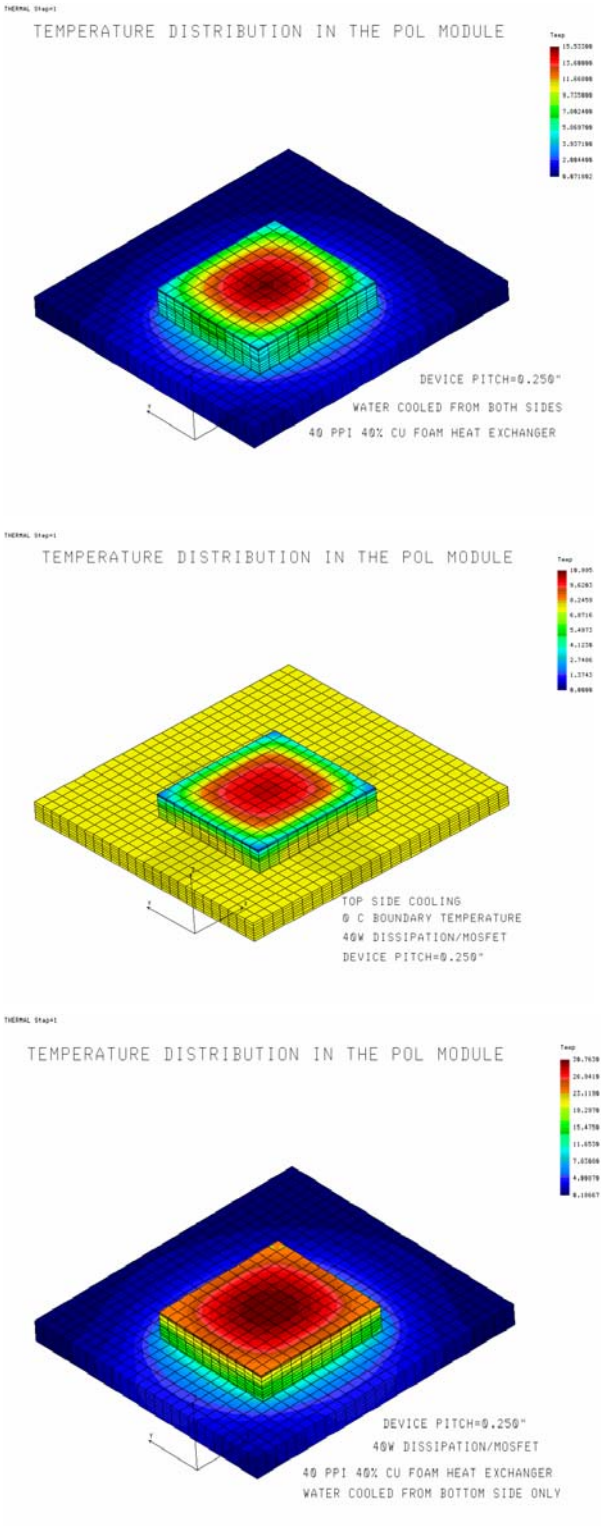

Figure 13. Temperature distribution in the POL module. Device pitch is 0.250" inch. The module is water cooled by a foam based integral heat exchanger from both sides (top), from top side only(middle) and from bottom side only (bottom.)

Average coolant temperature R_{ja} ($^oC/W$)

	Pitch=0.050"	Pitch=0.250"
Double	R_{ja}= 0.40	R_{ja}= 0.38
Top side	R_{ja}= 0.62	R_{ja}= 0.58
Bottom side	R_{ja}= 0.80	R_{ja}= 0.78

Fixed case temperature R_{jc} ($^oC/W$)

Double sided	R_{jc}= 0.20	R_{jc}= 0.20
Top side	R_{jc}= 0.30	R_{jc}= 0.25
Bottom side	R_{jc}= 0.48	R_{jc}= 0.48

Table 2. A summary of thermal performance POL module based on the results of the 3D FEA

RETICULATED METAL FOAM BASED INTEGRAL COMPACT HEAT EXCHANGER.

The integral, reticulated metal foam heat exchangers, Figure 14, offer low thermal resistance, high surface area and improved local transport characteristics (film coefficients) that help achieve the overall thermal performance levels shown above and in Figure 16 below (Ozmat, 1998).

The metal foam based heat exchangers offer great flexibility in designing for a given application prior to final assembly. This could be accomplished by the compression ratio in the xy plane (Leyda, 1990) that is perpendicular to the heat flux to be removed from the module base as shown in Figure 14. The compression effects the surface area flow resistance simultaneously in a predictable fashion (Ozmat, 1998). Since the compression also align the ligaments of the initially random cells the z axis thermal conductivity of the foam structure also increases thereby synergistically improving the thermal performance.

An another advantage of the reticulated metal foam is in the low xy modulus of the structure (Ashby 1983) which lowers the thermal stresses at the foam-ceramic interface allowing direct attachment without requiring a constraining surface sheet. This improves both the cost and the junction to ambient thermal resistance, Figure 15.

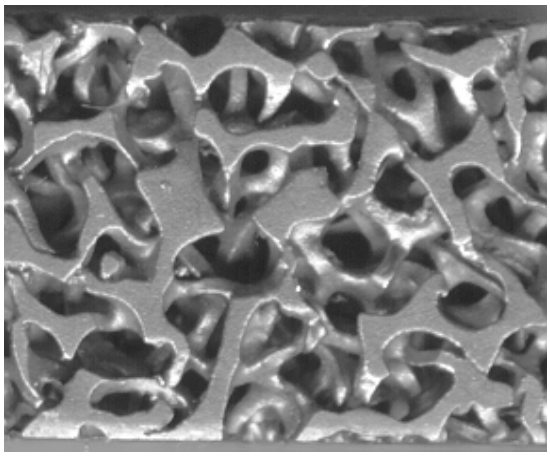

Figure 14. 10 ppi 8% dense foam compressed to 40% density. Direction of compression is perpendicular to the plane.

Figure 15. A 40 ppi ~ 40% dense reticulated Cu foam brazed to a Cu metalized AlN ceramic plate. Note that AlN and Cu metalization thickness are 0.040 inch and 0.003" whereas the foam thickness is 0.375 inch. The overall dimansions are, 1.800 inch x1.350x inch 0.375 inch.

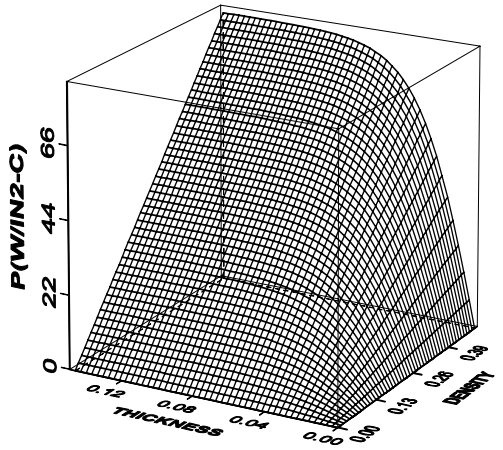

Figure 16. Thermal performance of a water cooled sytem using 40 ppi Cu foam.

In comparison with the other technologies, foam has a rather benign flow resistance that offers savings in the pump size and related energy loses while allowing higher flow rates to lower the junction temperatures in modules both as stand alone or in series.

CONCLUSIONS

The conclusions of the results of the FEA are summarized below:

The revolutionary POL technology using double sided, integral reticulated foam based high performance heat exchangers can handle up to 2500 W/in^2 heat fluxes at the chip level with 100 ^{o}C junction to ambient temperature rise.

The top sided cooling capability of POL improves the thermal resistance by more than 20% compare to bottom sided cooling only, and in the case of double sided cooling the improvement is more than 50 %.

Since the POL module technology uses only hard bonded interfaces rather than thermally conductive pastes and polymers, the junction to case thermal resistance is minimized and the effect of spreading becomes less important. Although, the advantages of heat spreading for thermal performance may not be debated, the low cost, low weight and reduced size requirements for advanced power module may be more readily achieved by integral heat exchangers than heat spreaders.

SUMMARY

A new approach to packaging high performance power devices was presented. It was shown that the GE's cost effective POL Power packaging technology is ideally suited for high heat flux and high performance applications. This is primarily due to the elimination of bond wires and the planar geometry which offers cooling of power devices from top, bottom or both sides of the power module. It was also shown that a cost effective, scaleable high performance integral heat exchanger can maximizes the thermal performance of POL technology thereby helping to utilize its full potential.

Due to the excellent thermal and electrical performance, low weight, volume, and cost effectiveness GE's revolutionary POL technology sets a new standard for the future of Packaging Power Electronics Modules.

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